Amendments to the Claims

1. (currently amended) A memory module, comprising:

an array of connections arranged in rows and columns such that there are first and second outer columns, the connections corresponding to electrical signals, and those connections in the first and second outer columns can be interchanged such that at least one of the electrical signals previously corresponding to at least one of the connections in the first outer column corresponds to at least one of the connections in the second outer column and at least one of the electrical signals previously corresponding to at least one of the connections in the second outer column corresponds to at least one of the connections in the first outer column.

2. (original) The memory module of claim 1, wherein the first outer column is a nearside column and the second outer column is a far-side column.

3. (original) The memory module of claim 1, wherein there are third and fourth outer columns having interchangeable connections.

4. (original) The memory module of claim 1, the memory module further comprising a package selected from the group comprised of: X16, and X4/X8.

5. (currently amended) A memory system, comprising:

a first memory module mounted on a first side of a substrate, the first memory module comprising:

an array of connections arranged in rows and columns such that there are first and second outer columns, the connections corresponding to signals, and that connections in the first and second outer columns can be interchanged such that at least one of the signals previously corresponding to at least one of the connections in the first outer column corresponds to at least one of the connections in the second outer column and at least one of the signals previously

corresponding to at least one of the connections in the second outer column corresponds to at least one of the connections in the first outer column;

a second memory module mounted on a second side of the substrate, comprising:

an array of connections arranged in rows and columns such that there are first and second outer columns, and that connections in the first and second outer columns can be interchanged;

a memory controller to control interchange of signals between first and second outer columns of the memory modules; and

signal traces in the substrate, wherein the connection in the first and second outer columns of the first and second memory modules are arranged such that signals routed on the traces have uniform routing lengths.

6. (original) The memory system of claim 5, the substrate further comprising a multi-layered printed circuit board.

7. (original) The memory system of claim 6, signal traces further comprising multiple signal traces in multiple layers of the printed circuit board.

8. (original) The memory system of claim 5, the memory modules being packaged in a package selected from the group comprised of: X16 and X4/X8.

9.-16. (canceled)

17. (new) The memory module of claim 1, wherein the interchanged connections in the first and second outer columns comprise connections corresponding to address signals.

18. (new) The memory module of claim 1, wherein the interchanged connections in the first and second outer columns comprise connections corresponding to bank address signals.

19. (new) The memory module of claim 1, wherein the interchanged connections in the first and second outer columns comprise connections corresponding to data signals within a byte lane.

20. (new) A memory system, comprising:

a first memory module mounted on a first side of a substrate, the first memory module comprising an array of connections arranged in columns such that there are first and second outer columns, wherein each of the connections corresponds to an electrical signal;

a second memory module, the second memory module comprising an array of connections arranged in columns such that there are first and second outer columns, wherein each of the connections corresponds to an electrical signal;

a memory controller to control interchange of signals between first and second outer columns of each of the memory modules; and

signal traces in the substrate.

21. (new) The system of claim 20, wherein the memory controller interchanges a first signal previously corresponding to a first connection in the first column of the second memory module with a second signal previously corresponding to a second connection in the second column of the second memory such that the first signal corresponds to the second connection and the second signal corresponds to the first connection.

22. (new) The system of claim 21, wherein the second memory module is mounted on a second side of the substrate.

23. (new) The system of claim 22, wherein at least one of the signal traces in the substrate connects the second connection with a third connection in the first column of the first memory module.

24. (new) The system of claim 23, further comprising at least one via completely penetrating the substrate, wherein the second connection is connected to the third connection through the via.

25. (new) The system of claim 23, wherein a length between a bus connection and the second connection is substantially uniform with a length between the bus connection and the third connection.

26. (new) The system of claim 21, wherein the first signal and the second signal are data signals within a byte lane.

27. (new) The system of claim 20, wherein the second memory module is stacked on the first memory module.

28. (new) The system of claim 20, wherein the second memory module further comprises third and fourth outer columns and electrical signals corresponding to connections in the third and fourth columns are interchangeable.